ABSTRACT OF THE DISCLOSURE

In a data communication circuit, data is multiplexed onto a communication link through multiple multiplexer stages and demultiplexed from the communication link through multiple demultiplexer stages in order that a clock signal applied to each multiplexing circuit need only be precisely distributed to a limited, high frequency portion of the circuit. Each circuit is clocked by a multiplying delayed locked loop bit clock generator. Where the number of parallel bits in the signal between the two stages is greater than two, the higher frequency stage coupled to the communication link is clocked by an N-phase overlapping clock. In the case of a multiplexer, the intermediate frequency signal is enabled in the higher frequency data multiplexer by concurrence of two clock phases.